Information Disclosure Statement

Applicant respectfully requests that a copy of the 1449 Form, listing all references that were submitted with the Information Disclosure Statement filed on August 28, 2001, marked as being considered and initialed by the Examiner, be returned with the next official communication.

§102 Rejection of the Claims

Claims 44, 60, 62-64, 66-68, 70-72, 74-77, 79-81, and 83 were rejected under 35 USC § 102(e) as being anticipated by Hu (U.S.5,725,739).

Applicant does not admit that Hu is indeed prior art, particularly with respect to material from U.S. Pat. No. 6,143,362 to which the present application claims priority. Applicant reserves the right to swear behind Hu at a later date. Applicant also notes that Hu and the present application are commonly assigned. Nevertheless the Applicant believes that the present invention is distinguishable from Hu for the following reasons.

The rejection states that:

> Hu teaches a metal filled high-aspect ratio contact comprising: . . . a titanium silicide layer 356 (titanium alloyed with silicon) within a high-aspect ratio contact opening 314 in the BPSG layer 312.

Hu appears to show titanium silicide layers 354 and 356 with different stoichiometries. However, Hu does not show a layer of a titanium alloy **covering the walls and bottom** of a contact hole, and a titanium silicide contact coupled to the layer.

In contrast, Applicant's independent claims, as amended, include a layer of a titanium alloy covering the walls and bottom of a contact hole, and a titanium silicide contact coupled to the layer. Among other advantages, Applicant submits that the structure in the present application where the titanium alloy layer covers the walls and bottom of a contact hole is possible due to the novel method described in the specification and claims, such as claim 83. As discussed in Applicant's background section on page 2, lines, 10-22,

> As device dimensions shrink, the contact holes become relatively deeper and narrower. Also, the walls of the contact holes become steeper, and closer to vertical. As a result, most metal deposition techniques form conductive layers having relatively small step coverage, and hence relatively high resistance. Step

> coverage is the ratio of the minimum thickness of a film as it crosses a step, to the nominal thickness of the film on flat regions, where thickness is generally measured perpendicular to the surfaces of the step and flat regions, and where the resultant value is usually expressed as a percentage. Thus, the effective contact resistance is increased at lower values of step coverage.

These, as well as other technical hurdles are overcome by applicant's novel process, thus making possible the novel structure as recited in the present claims.

Because the Hu reference does not show every element of Applicant's independent claims, a 35 USC § 102 rejection is not supported. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 44, 60, 64, 68, 72, 77, 81, and 83. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

Claims 44, 60, 62, 68, 71,72, 75-76, and 83 were rejected under 35 USC § 102(a/e) as being anticipated by Honeycutt (U.S. 5,644,166).

Applicant does not admit that Honeycutt is indeed prior art, particularly with respect to material from U.S. Pat. No. 6,143,362 to which the present application claims priority. Applicant reserves the right to swear behind Honeycutt at a later date. Applicant also notes that Honeycutt and the present application are commonly assigned. Nevertheless the Applicant believes that the present invention is distinguishable from Honeycutt for the following reasons.

The rejection states that "the device comprises . . . a titanium-germanium-silicide contact with a high aspect ratio contact hole in the BPSG layer 312." Honeycutt appears to show a titanium germanosilicide region 50. Honeycutt also appears to show a titnium germanide layer 52 coupled to walls of a contact opening. However, Honeycutt does not show a layer of a titanium alloy covering the walls **and bottom** of a contact hole, and a titanium silicide contact coupled to the layer.

In contrast, Applicant's independent claims, as amended, include a layer of a titanium alloy covering the walls and bottom of a contact hole, and a titanium silicide contact coupled to the layer.

Because the Honeycutt reference does not show every element of Applicant's independent claims, a 35 USC § 102 rejection is not supported. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 44, 60, 64, 68, 72, 77, 81, and 83. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

Claims 44-45 were rejected under 35 USC § 102(b) as being anticipated by Takemura (U.S. 5,534,716).

Applicant has amended claims 44 and 45 to include an element of a contact hole. Applicant respectfully submits that the Takemura reference does not include or suggest a contact hole as included in the amended claims.

Reconsideration and withdrawal of the 35 USC § 102(b) rejection is respectfully requested with respect to Applicant's claims 44 and 45.

<u>§103 Rejection of the Claims</u>

Claims 44, 60, 62-64, 66-68, 70-72, 74-77, 79-81, and 83 were rejected under 35 USC § 103(a) as being unpatentable over Honeycutt (U.S. 5,644,166) in view of Ajika (U.S. 5,049,975).

Honeycutt has been distinguished from the present application as detailed in arguments above. Applicant respectfully submits that Ajika does not cure the deficiencies of Honeycutt. Reconsideration and withdrawal of the 35 USC § 103(a) rejection is respectfully requested regarding claims 44, 60, 62-64, 66-68, 70-72, 74-77, 79-81, and 83.

Claim 83 was rejected under 35 USC § 103(a) as being unpatentable over Hu. Applicant respectfully submits that pursuant to arguments presented above, Hu does not support a 35 USC § 102 rejection.

Further, Applicant respectfully submits that Hu is not prior art as used in a 35 USC § 103 rejection with respect to selected material of the present application. Applicant notes that the Hu reference appears to be asserted under 35 USC § 102(e) with respect to material disclosed in US

Pat. No. 6,143,362. The present application was filed as a Continuation in Part Application Under 37 C.F.R. 1.53(b) on August 28, 2001, however the present application is entitled to a priority date of the parent Application (the '362 patent), filed on February 25, 1998. Hu was filed on July 8, 1996 and issued on March 10, 1998.

A reference asserted under 102(e) that was commonly owned with an application at the time the invention was made, cannot preclude patentability under 35 U.S.C. 103 when the application was filed on or after November 29, 1999. *35 U.S.C. 103(c); 1233 OG 55 (April 11, 2000).* The present application was filed on August 28, 2001, which is after November 29, 1999. Hu and the present application were, at the time the invention was made, owned by, or subject to an obligation of assignment to, the same entity.

Thus, Hu is commonly owned with the present application and is not prior art with respect to material disclosed in the parent application, US Pat. No. 6,143,362. Reconsideration and withdrawal of the 35 USC § 103(a) rejection is respectfully requested with respect to claim 83.

Allowable Subject Matter

Claims 61, 65, 69, 73, 78, and 82 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant acknowledges and thanks the Examiner for indication of allowability of claims 61, 65, 69, 73, 78, and 82. Pursuant to the arguments presented above, Applicant has not rewritten claims 61, 65, 69, 73, 78, and 82 in independent form at this time. Applicant respectfully submits that base claims 60, 64, 68, 72, 77, and 81 are in condition for allowance, thus removing the necessity to rewrite claims 61, 65, 69, 73, 78, and 82.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612- 373-6944) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

GURTEJ SINGH SANDHU ET AL.

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Date 10-18-02 By [signature]

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 18th day of October, 2002.

Name Amy Moriarty

Signature [signature]

Docket No. 303.676US2 Micron Ref. No. 97-0560.03
WD # 394499

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Clean Version of Pending Claims

CHEMICAL VAPOR DEPOSITION OF TITANIUM
Applicant: Gurtej Singh Sandhu et al.
Serial No.: 09/940,917

Claims 44-45 and 60-83, as of October 18, 2002 (date response to first office action filed).

Sub C1

44. (Amended) An integrated circuit comprising:

a layer of a titanium alloy covering the walls and bottom of a contact hole, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the layer.

45. The integrated circuit of claim 34, wherein the titanium alloy comprises titanium and zinc.

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60. (Amended) An integrated circuit comprising:

a semiconductor substrate;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy covering the walls and bottom of a contact opening in the insulating layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

61. The integrated circuit of claim 60, wherein the titanium alloy includes titanium and zinc.

62. The integrated circuit of claim 60, wherein the insulator layer includes silicon dioxide (SiO_2).

63. The integrated circuit of claim 60, wherein the electronic device includes a transistor.

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64. (Amended) An integrated circuit comprising:

a semiconductor substrate;

a transistor formed on the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy covering the walls and bottom of a contact opening in the insulating layer, the contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

65. The integrated circuit of claim 64, wherein the titanium alloy includes titanium and zinc.

66. The integrated circuit of claim 64, wherein the insulator layer includes silicon dioxide (SiO_2).

67. The integrated circuit of claim 64, wherein the contact opening includes a high aspect ratio contact opening.

68. (Amended) An integrated circuit comprising:

a semiconductor substrate;

an electronic device formed on the semiconductor substrate, the electronic device having an active region;

a borophosphous silicate glass (BPSG) layer over the active region;

an alloy layer of a titanium alloy covering the walls and bottom of a contact opening in the borophosphous silicate glass (BPSG) layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

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69. The integrated circuit of claim 68, wherein the titanium alloy includes titanium and zinc.

70. The integrated circuit of claim 68, wherein the electronic device includes a transistor.

71. The integrated circuit of claim 68, wherein the contact opening includes a high aspect ratio contact opening.

72. (Amended) An integrated circuit comprising:

a semiconductor substrate;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy covering the walls and bottom of a high aspect ratio

contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

73. The integrated circuit of claim 72, wherein the titanium alloy includes titanium and zinc.

74. The integrated circuit of claim 72, wherein the electronic device includes a transistor.

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75. The integrated circuit of claim 72, wherein the insulator layer includes silicon dioxide (SiO_2).

76. The integrated circuit of claim 72, wherein the insulator layer includes borophosphous silicate glass (BPSG).

77. (Amended) An integrated circuit comprising:

a semiconductor substrate;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy covering the walls and bottom of a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead,

arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

78. The integrated circuit of claim 77, wherein the titanium alloy includes titanium and zinc.

79. The integrated circuit of claim 77, wherein the insulator layer includes silicon dioxide (SiO_2).

80. The integrated circuit of claim 77, wherein the insulator layer includes borophosphous silicate glass (BPSG).

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81. (Amended) An integrated circuit comprising:

a semiconductor substrate;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

a borophosphous silicate glass (BPSG) layer over the source/drain region;

an alloy layer of a titanium alloy covering the walls and bottom of a high aspect ratio contact opening in the borophosphous silicate glass (BPSG) layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

82. The integrated circuit of claim 81, wherein the titanium alloy includes titanium and zinc.

83. (Amended) An integrated circuit comprising:

a semiconductor substrate;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy covering the walls and bottom of a contact opening in the insulating layer, the contact opening being at least partially over the active region, wherein the alloy layer is produced using a method including:

forming a seed layer supported by a substrate by combining a first precursor with a first reducing agent; and

forming the titanium layer supported by the substrate by combining a titanium-containing precursor with the seed layer.

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